REMARKS

Claims 1-21 are currently pending. No amendments are made in this paper. For at least the following reasons, Applicants respectfully submit that the presently pending claims are in condition for allowance.

Allowed Claims (11-19)

Applicants appreciate the indication that claims 11-19 are allowed and thank the Examiner for his work on this matter.

Claim Rejections under 35 U.S.C. § 112

Claims 1 and 20 were rejected as being indefinite under 35 U.S.C. § 112. More specifically, the Office Action states that the term "telescopic cascode arrangement" is a relative term which renders the claim indefinite. Claims 2-10 and 21 are rejected as being dependent on Claim 1. Claim 21 was also rejected as lacking antecedent basis. Each of the rejections under 35 U.S.C. § 112 is respectfully traversed.

Telescopic cascodes are well known in the art, and have been well-known for several decades. Accordingly, there is no need for the specification to explain what a telescopic cascode is. Moreover, determining what is a telescopic cascode and what is not a telescopic cascode is objectively determinable. Accordingly, one of ordinary skill in the art would be reasonably apprised of the scope the invention.

Throughout the discussion, it is understood that the scope of the words "gate", "drain", and "source" includes "base", "collector", and "emitter", respectively, and vice versa, since cascodes are equally applicable to field effect transistors and bipolar transistors.

The Office Action states, "from figure 2 the cascode arrangement is just a PMOS transistor (M1) connected in series with NMOS transistors (M0)". Applicants respectfully point out that this statement isn't quite correct. Figure 2 is a high-level drawing that does not illustrate any

one particular embodiment. Figure 2 does show a particular implementation of a keeper switch (namely, transistor M8), but does not show a particular implementation of a cascode arrangement, which is instead left generic in Figure 2. In Figure 2, transistor M0 is not shown as being either a PMOS transistor or an NMOS; rather, the polarity of transistor M0 is left unspecified (no little "arrow" is shown).

Also, in Figure 2, it is not specified whether a telescopic cascode or another type of cascode is being used. In Figure 2, it is not specified whether transistor M0 is in series with M1 or not. Figure 2 does not show a particular cascode. The focus of Figure 2 is on the cascode transistor M1 and the keeper switch transistor M8. Figure 2 indicates that the cascode transistor M1 is a cascode transistor which is part of a cascode that includes at least one other transistor (M0), but the details of transistor M0 and the details of the connection of transistor M0 to transistor M1 is not shown because Figure 2 is a high-level drawing which represents many different embodiments in which the details of transistor M0 and the connections of transistor M0 vary from embodiment to embodiment.

Figures 3-7 show examples of particular cascodes. In Figures 3 and 4, transistors M6 and transistor M2 form a telescopic cascode, in which transistor M2 is a cascode transistor. Transistors M6 and M2 are coupled in series, with the **source** of transistor M2 coupled to the **drain** of transistor M2. Also, transistors M7 and M3 form another telescopic cascode, where transistor M3 is a cascode transistor. Transistors M2 is a cascode transistor, and transistor M3 is a cascode transistor. However, transistors M2 and M3 do not form a cascode with each other; rather, they are each part of a **separate** cascode.

In Figures 5-7, transistors M11 and M2 form a telescopic cascode, transistors M12 and M4 form a telescopic cascode, transistors M13 and M3 form a telescopic cascode, and transistors M14 and M5 form a telescopic cascode.

In a telescopic cascode arrangement of two transistors, the telescopic cascode includes a first transistor, and a cascode transistor that is coupled in series with the first transistor. The **source** of

the cascode transistor is coupled to the **drain** of the first transistor. To form a telescopic cascode, it is not sufficient that two transistors be connected in series. If two transistors are connected in series with the **drain** of one of the two transistors directly connected to the **drain** of the other, this is not a cascode, even though the two transistors are connected in series.

Claim 21 was also rejected as the limitation "the second transistor" lacking antecedent basis. (The Office Action actually refers to Claim 22, which does not exist; it is assumed that the Office Action meant to refer to Claim 21). Claim 21 depends from Claim 1, which provides antecedent basis for the second transistor at line 2 of Claim 1.

For at least the reasons stated above, it is respectfully submitted that all of the rejections to Claims 1, 2-10, 20, and 21 under 35 U.S.C. § 112 should be withdrawn.

Claim Rejections under 35 U.S.C. § 102

Claims 1-8 were rejected under 35 U.S.C. § 102(e) as being anticipated by Prodanov (6,693,469). Claims 1, 9-10, and 20 were rejected under 35 U.S.C. 102(b) as being anticipated by Annema et al. (6,320,414). Each of the rejections is respectfully traversed.

It is respectfully submitted that the rejections under 35 U.S.C. § 102 to Claim 1 should be withdrawn at least because neither Prodanov nor Annema discloses, "a telescopic cascode arrangement", in conjunction with the other limitations of Claim 1.

In a telescopic cascode arrangement of two transistors, the telescopic cascode includes a first transistor, and a cascode transistor that is coupled in series with the first transistor, with the source of the cascode transistor coupled to the drain of the first transistor. To form a telescopic cascode, it is not sufficient that two transistors be connected in series. If two transistors are connected in series with the drain of one of the two transistors directly connected to the drain of the other, this is not a cascode, even though the two transistors are connected in series.

Applicants note that, in FIG. 21 of Annema, transistors T2 and T3 form a telescopic cascode, and that transistors T*2 and T*3 form another telescopic cascode. However, transistors T2 and Tb6 do not form a telescopic cascode.

Similarly, in FIG. 4 of Prodanov, transistors P5 and N5 do not form a telescopic cascode. The drain of P5 is connected to the drain of transistor N5.

For at least the reasons stated above, it is respectfully submitted that the rejections to Claim 1 under 35 U.S.C. § 102 should be withdrawn.

Further, it is respectfully submitted that the rejection under 35 U.S.C. § 102 to Claim 20 should be withdrawn at least because Annema does not disclose, "a telescopic cascode configuration" in conjunction with the other elements of Claim 20.

It is respectfully submitted that the rejection(s) under 35 U.S.C. § 102 should be withdrawn with respect to Claims 2-10 and 21 at least because Claim 1 is allowable.

Further, it is respectfully submitted that the rejection to Claim 8 should be withdrawn at least because Prodanov does not disclose, "the second transistor is one of a group consisting of an n-type transistor and the p-type transistor, and the keeper transistor is the other of the group consisting of the n-type transistor and the p-type transistor", as recited in Applicants' Claim 8. According to the Office Action, Prodanov shows a circuit that meets all of the limitations of Claim 1-8, where the first transistor is N5, the second transistor is P5, and the keeper switch circuit is P4. The Office Action states that (7) Prodanov shows that the second transistor P5 is one of a group consisting of an n-type transistor and a p-type transistor, and the keeper transistor P4 is the one of the group consisting of the n-type transistor and the p-type transistor. Further, the Office Action states that (8) Prodanov shows that the second transistor P5 is one of a group consisting of an n-type transistor and the p-type transistor, and the keeper transistor P4 is the other of the group consisting of the n-type transistor and the p-type transistor.

However, it is impossible for transistors P5 and P4 to meet the limitations of both claims. Claim 7 requires that either: the second transistor and the keeper transistor are both p-type transistors, or that the second transistor and the keeper transistor are both n-type transistors. Claim 8 requires that either: the second transistor is a p-type transistor and the keeper transistor is an n-type transistor, or that the second transistor is an n-type transistor and the keeper transistor is a p-type transistor.

Transistors P5 and P4 are both p-type transistors. Therefore, they do not meet the limitations of Claim 8.

CONCLUSION

It is respectfully submitted that each of the presently pending claims (Claims 1-21) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicant's representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

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